APPARATUS AND METHOD OF WORDLINE/BITLINE REDUNDANCY CONTROL USING SHIFT REGISTERS IN AN SRAM

ABSTRACT OF THE DISCLOSURE

A decoder for use in wordline/bitline redundancy control is disclosed. In one aspect, the decoder includes first and second wordlines respectively coupled to redundant first and second wordlines, where the first and second wordlines are configured to be activated based on decoded first and second addresses. In addition, the decoder includes first and second shift registers respectively coupled to the redundant first and second wordlines, where each is configured to respectively activate the redundant first and second wordlines when the first or second wordlines contain a defect. In addition, a method of selecting wordlines for use in wordline/bitline redundancy control and a wordline decoder having redundancy control capabilities are also disclosed.